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A GAIN CONTROL CIRCUIT, AND A RADIO COMMUNICATION APPARATUS USING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a gain control circuit and a radio communication apparatus using such gain control circuit, and more particularly—the present invention relates to ~~the~~ a gain control circuit to be used for an output power control in a mobile radio communication apparatus, and to ~~the~~ a radio communication system using such mobile radio communication apparatus.

2. Description of the Related Art

In a mobile radio communication system, for example, in a mobile telephone system, it is desirable that ~~an~~ the output power of each mobile terminal is controlled so as to be received with the same signal strength at a base station, in order to increase ~~a~~ the communication capacity of the base station.

In particular, in ~~a~~ communication system, in which the mobile telephone system employs a spectrum scattering method referred to as a CDMA (Code Division Multiple Access) system, plural stations are assigned to the same frequency band, and a received signal is recovered by means of a predetermined scattering code. And accordingly, ~~an~~ output power control of each mobile terminal becomes a necessary requirement.

There are two types of power control systems that perform the output power control of the mobile terminal. One of the two types of ~~the~~ systems is to determine the output power of the mobile terminal in accordance with ~~the~~a signal strength of a received signal by the mobile terminal, wherein the signal is transmitted from the base station. This type depends on the hypothesis that there is a strong correlation between ~~a~~the signal propagation from the base station to the mobile terminal and ~~the~~a signal propagation from the mobile terminal to the base station. This type of control is named ~~as~~ an open loop control.

The other ~~one~~ type of system is to determine ~~by~~for information about an actually received ~~signal~~the strength of the radio wave at the base station, wherein such information is

transmitted from the base station to the mobile terminal. This type of control is named ~~as~~ a closed- loop control.

A gain control circuit is necessary in order to control the output power. ~~As~~ The performances of such gain control circuit requires a wide gain control range, a wide dynamic range, a good controllable linearity, an absolute gain accuracy, a good temperature characteristic and a broad frequency band.

For example, as the gain control range, ~~about~~ a gain of about 90 dB is necessary in a receiving side, and ~~about~~ a gain of about 80 dB is necessary in a transmitting side. As for the dynamic range, it is necessary to consider, particularly in the receiving side, a situation where ~~a~~ the radio signal wave ~~to be~~ received is very weak ~~but~~and a strong interfering radio wave enters. And accordingly, as for the gain control circuit, ~~a~~ tolerance to a very large input signal and a low noise characteristic are simultaneously required.

It is necessary to match the characteristic of the receiving side gain control circuit and the transmitting side gain control circuit about the controllable linearity, the absolute gain accuracy, the temperature characteristic in order to raise ~~an~~ the accuracy of the previously described the open loop control. About the frequency bandwidth, it is different by a system, but it is ~~the~~ easiest to do such an operation by an IF (Intermediate Frequency) stage. As for the typical frequency of that purpose, there are many cases that are around 100MHz.

FIG.6 is a circuit diagram which shows a conventional embodiment of a variable gain circuit constituting a gain control circuit. The variable gain circuit of this conventional embodiment has a differential amplifying circuit 101, a bias circuit 102, a pair of current dividing circuits 103 and 104 and a pair of resistive circuit meshes 105 and 106.

The differential amplifying circuit 101 comprises npn- type differential pair transistors Q101 and Q102, in which each emitter electrode of the transistors Q101 and Q102 is grounded through respective emitter resistors R101 and~~,~~ R102, respectively ~~.~~ An input voltage Vi is supplied to input terminals Vin +, Vin- connected to each base electrode of the differential pair transistors Q101 and Q102.

The bias circuit 102 comprises bias resistors R103 and R104 connected to each base electrode of the differential pair transistors Q101 and Q102 and a bias voltage supply 107

connected between the bias resistors R103 and R104 and the ground ~~for supplying~~and which supplies a fixed bias voltage Vbias to each base electrode of the differential pair transistors Q101 and Q102 through the bias resistors R103 and R104.

One current dividing circuit 103 comprises npn~~-~~ type differential pair transistors Q103 and Q104, in which each emitter electrode of the transistors Q103 and Q104 is connected commonly to a collector electrode of the transistor Q101. The other current dividing circuit 104 comprises npn~~-~~ type differential pair transistors Q105 and Q106, in which each emitter electrode of the transistors Q105 and Q106 is connected commonly to a collector electrode of the transistor Q102.

In these current dividing circuits 103 and 104, each base electrode of transistors Q103 and Q105 ~~are~~ is connected to each other, each base electrode of transistors Q104 and Q106 ~~are~~ is connected to each other and a control voltage Vc is applied to a pair of input terminals Vc+, Vc- connected between these base electrodes of the transistors Q103, Q105, Q104 and Q106. And, an output voltage Vo is provided from a pair of output terminals Vout+, Vout- connected to each collector electrode of the transistors Q103 and Q105.

~~The o~~One resistive circuit mesh 105 comprises resistors R105 and R106 connected between the differential pair transistors Q103, Q104 and a power source voltage VCC and a resistor R107 connected to the collector electrodes of the differential pair transistor Q103 and Q104. The other resistive circuit mesh 106 comprises resistors R108 and R109 connected between the differential pair transistors Q105, Q106 and the power source voltage VCC and a resistor R110 connected to the collector electrodes of the differential pair transistor Q105 and Q106.

~~A~~ The transmission gain G of the variable gain circuit, as shown in Fig. 6, is now explained. At first, the control voltage Vc from the control voltage supply circuit 108 is supplied to the input terminals Vc+, Vc- connected between the base electrodes of the differential pair transistors Q103 and Q104 and the base electrodes of the differential pair transistors Q105 and Q106. This control voltage supply circuit 108 generates an internal control voltage Vc varying in linearity relative to the external control voltage VC supplied from an external control voltage generating source 109.

The transmission gain G varies by changing ~~a~~ the ratio of flowing currents of the current dividing circuits 103 and 104 in accordance with the internal control voltage Vc generated at the control voltage supply circuit 108 based on ~~the external~~the external control voltage VC from the external control voltage generating source 109, wherein ~~a~~ the potential difference $\triangle$Vbe between base electrodes of the differential pair transistors Q103 and Q104 and the differential pair transistors Q105 and Q106 are changed by means of the internal control voltage Vc supplied from the control voltage supply circuit 108.

The transmission gain G is expressed by ~~a~~ the next expression:~~.~~

$$G = Gmax /\{1+ \exp (-qVc/kt)\}+Gmim/\{1+ \exp (qVc/kt)\}$$

~~The~~ Gmax shows ~~a~~ the maximum transmission gain of the variable gain circuit, ~~the~~ Gmin shows ~~a~~ the minimum transmission gain of the variable gain circuit, ~~the~~ q shows ~~a~~ the charge of an electron, ~~the~~ k shows the Boltzmann's constant and ~~the~~ t shows ~~an~~ the absolute temperature.

As described above, in the conventional variable gain circuit, the transmission gain G is controlled by means of the internal control voltage Vc that varies in linearity relative to the external control voltage VC. As shown in Fig. 7, as ~~a gain control characteristic to~~ the external control voltage VC approaches ~~to~~ the maximum transmission gain Gmax or the minimum transmission gain Gmin, ~~a~~ the characteristic curve tends to bend, and ~~a~~ the linearity of the variable gain circuit becomes deteriorated.

This kind of variable gain circuit composes a gain control circuit by providing a plural number of the variable gain circuits in a cascade connection by way of buffer circuits. For example, this kind of gain control circuit is used as an AGC (Automatic Gain Control) amplifier for amplifying an IF (Intermediate Frequency) signal of a transmission stage in an RF (Radio Frequency) front-end section of the CDMA~~-~~ type mobile telephone apparatus.

In such an application, ~~sucha~~ multistage~~-~~ type variable gain circuit, such as mentioned above, is used as the AGC amplifier in order to satisfy a request for a wide variable gain range, but if thea linearity of the gain control characteristic is bad, it is necessary to increase the number of stages of the variable gain circuit to be cascade-connected thereto. As a result, athe circuit scale of the AGC amplifier becomes

large and ~~a~~ current consumption increases~~,~~ too.

SUMMARY OF THE INVENTION

A primary object of the invention is to provides a gain control circuit having a ~~better~~more controllable linear characteristic relative~~related~~ to the~~an~~ external control voltage and a radio communication apparatus using such gain control circuit.

The~~A~~ gain control circuit of the present invention comprises a variable gain circuit having a predetermined gain control range and a control voltage supply circuit for supplying an internal control voltage to the variable gain circuit as a gain control signal, wherein the control voltage supply circuit generates the internal control voltage in response to an external control voltage as to compensate ~~a~~the linearity of the variable gain circuit to ~~an~~the extent of the external control voltage where the variable gain circuit loses ~~a~~ linearity. And, this gain control circuit can be used at an IF signal amplifying stage of a radio communication apparatus, such as a mobile telephone ~~apparatuse~~apparatus,~~s~~ as an amplification means.

Namely, in a radio communication apparatus having an amplification means in a transmitting stage for amplifying an intermediate frequency signal and supplying the intermediate frequency signal to a mixing circuit, according to another aspect of the present invention, the amplification means comprises a variable gain circuit having a predetermined gain control range and a control voltage supply circuit for supplying an internal control voltage to the variable gain circuit as a gain control signal, wherein the control voltage supply circuit generates the internal control voltage in response to an external control voltage so as to compensate ~~a~~ the linearity of the variable gain circuit to ~~an~~ the extent of the external control voltage where the variable gain circuit loses ~~a~~ linearity.

Compensation of the non-linearity is done in a range where ~~a~~ the linearity of gain control characteristic is lost. As a result, the linear range of the variable gain circuit can be expanded, so that the linearity extends to the range where linearity is conventionally lost in the gain control characteristic of a gain control circuit.

BRIEF DESCRIPTION OF THE DRWAINGS

In the accompanying drawings:

Fig. 1 is a circuit diagram showing a construction of a gain control circuit related to a first embodiment of the present invention;

Fig. 2 is a circuit diagram showing a concrete circuit structure of an example of a variable gain circuit;

Fig. 3A is a graph chart of an internal control voltage ~~as to~~versus an external control voltage;

Fig. 3B is a graph chart showing a characteristic of a transmission gain ~~as to~~versus the external control voltage;

Fig. 4 is a block diagram showing a construction of a gain control circuit related to a second embodiment of the present invention;

Fig. 5 is a block diagram showing an example of a construction of ~~an~~ RF front- end part in a CDMA- type mobile telephone apparatus;

Fig. 6 is a circuit diagram showing a construction of a gain control circuit related to a conventional embodiment; and

Fig. 7 is a graph chart of an external control voltage - transmission gain related to the conventional embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Detailed descriptions of preferred embodiments of the present invention are described with reference to the accompanying drawings as follows. Fig. 1 is a circuit diagram showing a construction of a gain control circuit related to a first embodiment of the present invention.

A gain control circuit, according to the present invention, comprises a variable gain circuit 11 having a limited variable gain range and a control voltage supply circuit 13, wherein the control voltage supply circuit 13 receives an external control voltage VC from an external control voltage generating source 12 and converts this external control voltage VC into an internal control voltage Vc to be supplied to the variable gain circuit 11 as a gain

control voltage.

As the variable gain circuit 11, a circuit having the same circuit construction as the variable gain circuit related to the conventional embodiment shown in Fig. 6 is used. In other words, the variable gain circuit 11 comprises a differential amplifying circuit 21, a bias circuit 22, a pair of current dividing circuits 23 and 24 and a pair of resistive circuit meshes 25 and 26, as shown in Fig. 2.

The differential amplifying circuit 21 comprises npn- type differential pair transistors Q21 and Q22, wherein emitter electrodes of the differential pair transistors Q21 and Q22 are commonly connected to the ground by way of emitter resistors R21 and R22, and an input voltage Vi is supplied to each base electrode of the differential pair transistors Q21 and Q22 by way of a pair of input terminals Vin+ and Vin-.

The bias circuit 22 comprises bias resistors R23 and R24 connected respectively to the base electrodes of the differential pair transistors Q21 and Q22 and a bias voltage supply 27 connected between the bias resistors R23 and R24 and the ground so as to supply a bias voltage Vbias to each base electrode of the differential pair transistors Q21 and Q22 through the bias resistors R23 and R24.

The one current dividing circuit 23 comprises npn- type differential pair transistors Q23 and Q24, wherein each emitter electrode of the differential pair transistors Q23 and Q24 is connected commonly to a collector electrode of the transistor Q21. The other current dividing circuit 24 comprises npn- type differential pair transistors Q25 and Q26, wherein each emitter electrode of the differential pair transistors Q25 and Q26 is connected commonly to a collector electrode of the transistor Q22.

In these current dividing circuits 23 and 24, base electrodes of the transistors Q23 and Q25 are connected to each other and base electrodes of the transistors Q24 and Q26 are connected to each other, wherein the internal control voltage Vc is applied to these base electrodes of the transistors Q23, Q25, Q24 and Q26 by way of input terminals Vc+ and Vc-. And, an output voltage Vo is derived from collectors of the transistors Q23 and Q25 by way of a pair of output terminals Vout+ and Vout-.

The one resistive circuit mesh 25 comprises resistors R25 and R26 connected

between the differential pair transistors Q23 and Q24 and a power source voltage VCC and a resistor R27 connected between the collector electrodes of the differential pair transistors Q23 and Q24. The other resistive circuit mesh 26 comprises resistors R28 and R29 connected between the differential pair transistors Q25 and Q26 and the power source voltage VCC and a resistor R30 connected between the collector electrodes of the differential pair transistors Q25 and Q26.

In the variable gain circuit 11, as constructed above, the internal control voltage Vc is supplied not only between the base electrodes of the differential pair transistors Q23 and Q24 but also between the base electrodes of the differential pair transistor Q25 and Q26, wherein the internal control voltage Vc is generated in the control voltage supply circuit 13 based on the voltage control at the external control voltage generating source 12. And ~~a~~ the gain varies based on ~~a~~ the change of current allocation at the current dividing circuits 23 and 24 in response to this internal control voltage Vc.

On the other hand, the control voltage supply circuit 13 generates the internal control voltage Vc in response to the external control voltage VC, wherein the internal control voltage Vc compensates ~~an~~ non-linearity of the gain control characteristic of the variable gain circuit 11 in ~~an~~ non-linear range. To be more concrete, in both ranges that are less than and greater than the linear range of the gain control characteristic in the conventional variable gain circuit, as shown in a dotted line in Fig. 3B, the control voltage supply circuit 13 generates the internal control voltage Vc shown in Fig. 3A by a solid line having ~~a~~ more change relative to the external control voltage VC than the conventional internal control voltage beyond the linear range.

In the following, a concrete construction of the control voltage supply circuit 13 is described with reference to Fig. 1, wherein the external control voltage VC given by the external control voltage generating source 12 is supplied to a first and a second differential circuits 15 and 16 by way of a buffer circuit 14 and is further supplied to a current-voltage converting circuit 18 by way of a buffer circuit 17.

The first differential circuit 15 comprises pnp- type differential pair transistors Q11 and Q12 respectively having emitter electrodes commonly connected to each other and a

current source I-11 connected between the commonly connected emitter electrodes of the transistors Q11 and Q12 and the power source voltage VCC. And, in the first differential circuit 15, a base electrode of the transistor Q11 is supplied with a reference voltage Vk1, which corresponds to thea lower limit of the linear range in the gain control characteristic of the conventional one as shown in Figs. 3A and 3B, and a base electrode of the transistor Q12 is supplied with the external control voltage VC by way of the buffer circuit 14.

In this the first differential circuit 15, a collector electrode of the transistor Q11 is connected directly to the ground GND, and a collector electrode of the transistor Q12 ~~is~~ ~~alsoalso~~ is connected to the ground GND by way of a diode-connected npn- type transistor Q13 and a resistor R11. The transistor Q13 constitutes a current mirror circuit together with an npn- type transistor Q14, wherein a base electrode of the transistor Q13 is connected to a base electrode of the transistor Q14 and an emitter electrode of the transistor Q14 is connected to the ground GND by way of a resistor R12.

The second differential circuit 16 comprises npn- type differential pair transistors Q15 and Q16 respectively having emitter electrodes commonly connected to each other and a current source I-12 connected between the commonly connected emitter electrodes of the transistors Q15 and Q16 ~~and theand~~ the ground GND. And, in the second differential circuit 16, a base electrode of the transistor Q15 is supplied with a reference voltage Vk2, which corresponds to an upper limit of the linear range in the gain control characteristic of the conventional one as shown in Figs. 3A and 3B, and a base electrode of the transistor Q16 is supplied with the external control voltage VC by way of the buffer circuit 14.

In this the second differential circuit 16, a collector electrode of the transistor Q15 is connected directly to the power source voltage VCC, and a collector electrode of the transistor Q16 ~~is alsoalso~~ is connected to the power source voltage VCC by way of a diode-connected pnp- type transistor Q17 and a resistor R13. The transistor Q17 constitutes a current mirror circuit together with an pnp- type transistor Q18, wherein a base electrode of the transistor Q17 is connected to a base electrode of the transistor Q18 and an emitter electrode of the transistor Q18 is connected to the power source voltage VCC by way of a resistor R14.

On the other hand, the current-voltage converting circuit 18 comprises an npn- type transistor Q16 having an emitter electrode connected to an output (here-in-after referred to as a node A) of the buffer circuit 17, a resistor 15 interposed between a collector electrode of the transistor Q16 and the power source voltage VCC, a series-connected resistor R16 and direct-current power source 19 and a current source I-13 interposed between the node A and the ground GND. Further, each collector electrode of the transistors Q14 and Q18 of the two current mirror circuits is connected to the node A.

~~A~~ The circuit operation of the control voltage supply circuit 13 is described with reference to Fig. 3A and Fig. 3B. In the figures, Fig. 3A shows a graph chart of the internal control voltage Vc ~~as to~~versus the external control voltage VC and Fig. 3B shows a graph chart showing ~~a~~ the characteristic of the~~a~~ transmission gain G ~~as~~ versus~~to~~ the external control voltage VC.

At first, when the external control voltage VC external control voltage generating source 12 is in the voltage range from the reference voltage Vk1 of the first differential circuit 15 to the reference voltage Vk2 of the second differential circuit 16, a~~the~~ current proportional to the external control voltage VC flows through the resistor R16 by way of buffer circuits 14 and 17 in the current-voltage converting circuit 18. Then a voltage at the collector electrode of the transistor Q16 generated according to this current is supplied to a variable gain circuit 11 as an internal control voltage Vc.

In other words, as shown in Fig. 3A by a solid line, a~~the~~ internal control voltage Vc proportional to the external control voltage VC is to be generated in the voltage range between Vk1 and Vk2 of the external control voltage VC. Accordingly, the gain of the variable gain circuit 11 is changed linearly relative to the external control voltage VC by supplying thus generated internal control voltage, Vc to the variable gain circuit 11 as the control voltage as shown in Fig. 3B by a solid line.

As shown by a dotted line in Fig. 3A, the internal control voltage Vc of a conventional circuit which varies in linearity relative to the external control voltage VC in the voltage range less than the reference voltage Vk1 and more than the reference voltage Vk2 is obtained from the current-voltage converting circuit 18 and is supplied to the variable gain

circuit 11. Thereby, the gain control characteristic of the variable gain circuit 11 ~~is~~ deteriorate~~s~~d in the linearity as the gain control characteristic approaches and exceeds ~~to~~ the Gmax and the Gmin, as shown in Fig. 3B by a dotted line.

In the gain control circuit of this embodiment of the present invention, when the external control voltage VC becomes less than the reference voltage Vk1 of the first differential circuit 15, the transistor Q12 ~~becomes~~ enters the ON state, then current from the current source I-11 flows to the transistor Q13 by way of the transistor Q12. As the transistor Q13 constitutes the current mirror circuit with the transistor Q14, so that if each characteristic of the transistors Q13 and Q14 is equal and if each resistive value of the resistors R11 and R12 is equal, then ~~the~~ a current having the same value as the current flowing through the transistor Q13 flows through the transistor Q14.

At this moment, the transistor Q18 is in the off state and the collector electrode of the transistor Q14 is connected to the node A, and accordingly the current flowing into the transistor Q14 is supplied by the current-voltage converting circuit 18. Thereby in the current-voltage converting circuit 18, ~~a~~the change of the collector potential of the transistor Q16 becomes large relative to the external control voltage VC, because the current by the transistor Q14 flows through the transistor Q16 in addition to the current from the current source I13 and the current flowing through the resistor R16.

Therefore, in the voltage range where the external control voltage VC is less than the reference voltage Vk1, ~~a~~the reduction rate of the internal control voltage Vc becomes larger than the reduction rate of the internal control voltage Vc of the voltage range between Vk1 and Vk2 as the external control voltage VC goes low. And by applying the internal control voltage Vc having the large changing rate to the variable gain circuit 11, the linearity of the gain control characteristic can be extended to near the minimum transmission gain Gmin as shown in Fig. 3B.

On the other hand, the transistor Q16 ~~becomes~~ enters the ON state when the external control voltage VC exceeds the reference voltage Vk2 of the second differential circuit 16. Therefore, current flows to the current source I12 through the transistors Q16 and Q17. As the transistor Q17 composes the current mirror circuit with the transistor Q18, so that if each

characteristic of the transistors Q17 and Q18 is equal and each resistive value of the resistors R13 and R14 is equal, then current ~~having~~ the same as current flowing in the transistor Q17 flows through the transistor Q18.

At this moment, the transistor Q14 is in the off state and the collector electrode of the transistor Q18 is connected to the node A, and accordingly the current flowing through the transistor Q18 is supplied to the current-voltage converting circuit 18. Thereby, in the current-voltage converting circuit 18, ~~a~~ the change of the collector potential of the transistor Q16 becomes large relative to the external control voltage VC, because the current by the transistor Q18 flows through the transistor Q16.

Therefore, in the voltage range where the external control voltage VC ~~is~~ exceeds the reference voltage Vk2, ~~a~~ the increasing rate of the internal control voltage Vc becomes larger than the increasing rate of the internal control voltage Vc of the voltage range between Vk1 and Vk2 as the external control voltage VC goes lower. And, by applying the internal control voltage Vc having the large changing rate to the variable gain circuit 11, the linearity of the gain control characteristic can be extended to near the maximum transmission gain Gmax, as shown in Fig. 3B.

As described above, the control voltage supply circuit 13 generates a mid- range part of the internal control voltage Vc varying linearly against the external control voltage VC to the voltage range between Vk1 and Vk2, and a higher range part and a lower range part of the internal control voltage Vc varying in higher rate against the external control voltage VC to a voltage range outside of the voltage range between Vk1 and Vk2. And, thus generated internal control voltage Vc is supplied to the variable gain circuit 11, and accordingly the linearity can be compensated in the range where the linearity is lost in the conventional circuit shown in ~~the~~ Fig. 3B by the dotted line.

As a result, ~~a~~ the linearity for the gain control characteristic of the variable gain circuit 11 is improved against the external control voltage VC, so that ~~an~~ the usable linear range of the variable gain circuit 11 can be expanded, as shown in Fig. 3B by the solid line.

FIG.4 is a block diagram showing a construction of a gain control circuit related to a second embodiment of the present invention.

The gain control circuit related to the embodiment comprises a plurality of cascade-connected variable gain circuits 31, 32 and 33, each having differential input and output, and a control voltage supply circuit 35 to supply internal control voltages Vc1, Vc2 and Vc3 to the variable gain circuits 31, 32 and 33, respectively, wherein these internal control voltages Vc1, Vc2 and Vc3 are generated based on a given external control voltage VC from an external control voltage generating source 34.

Each of variable gain circuits 31, 32 and 33 has a limited variable gain range, and is connected mutually by way of buffer circuits 36 and 37. These variable gain circuits 31, 32 and 33 have gain control terminals VC 1, VC 2 and VC 3, respectively, and the internal control voltages Vc1, Vc2 and Vc3 set in the control voltage supply circuit 35 are supplied to these gain control terminals VC 1, VC 2 and VC 3 as gain control voltages, as shown in Fig. 4.

In the gain control circuit of the second embodiment of the invention, the variable gain circuit shown in Fig. 2 is used as each of the variable gain circuits 31, 32 and 33. Namely the gain control circuit having the wide gain control range is composed by cascade-connectinged these variable gain circuits 31, 32 and 33. In this gain control circuit, the variable gain circuit 31 handles the lower range, the variable gain circuit 32 handles the mid-range and the variable gain circuit 33 handles the upper range on the linearity curve shown in Fig. 3B.

In addition, the circuit structure of the control voltage supply circuit 13 shown in Fig. 1 is used as the control voltage supply circuit 35. In the characteristic of the external control voltage VC against the internal control voltage Vc shown in Fig. 3A, the internal control voltages Vc1, Vc2 and Vc3 obtained from the control voltage supply circuit 35 have offset value and are supplied to each of the variable gain circuits 31, 32 and 33.

As described above, the internal control voltages Vc1, Vc2 and Vc3 obtained from the control voltage supply circuit 35 are supplied to the variable gain circuits 31, 32 and 33 as the gain control voltage which compensates the non-linearity of upper and lower ranges by the variable gain circuits 31, 32 and 33.

As thus described, in the present invention, the variable gain circuits 31, 32 and 33

are cascade-connected, the internal control voltages Vc1, Vc2 and Vc 3 are generated so as to compensate the non-linearity of a gain control circuit having relatively wide gain control range, and thus generated internal control voltage Vc1, Vc2 and Vc 3 are supplied to each of the variable gain circuits 31, 32 and 33. Accordingly, each ~~of~~ linearity characteristic of the variable gain circuits 31, 32 and 33 is improved, and thereby total linearity of the gain control circuit is largely improved as shown in Fig. 3B by the solid line.

On the contrary, when the linear range of the gain control characteristic for the gain control circuit is not so wide as compared with the conventional linear range, only two variable gain circuits, for example the variable gain circuits 32 and 33, are necessary to expand the linear range of the gain control characteristic.

In this case, the power consumption for the AGC amplifier is reduced for the sake of this. Further if the gain control circuit comprises two variable gain circuits, one of buffer circuits 36 and 37 ~~is also~~also is omitted and further saving of the power consumption and a reduction of circuit volume are expected.

In addition, the gain control circuit in Fig. 4 comprises three cascade-connected ~~three~~ variable gain circuits~~,~~; however, the number of the variable gain circuits is not limited to three, and it is possible to use four or more ~~of~~ variable gain circuits in order to expand the linearity range of the gain control circuit.

The gain control circuit of the above-described second embodiment is used, for example, as a gain control circuit ~~of an~~for a RF front-end part in a CDMA- type mobile telephone apparatus. FIG.5 is a block diagram showing one example of a construction of the RF front-end part in the CDMA- type mobile telephone apparatus.

A radio wave received as a receiving RF signal by ~~an~~ radio antenna 41 is supplied to a mixer circuit 44 by way of a frequency band separation filter 42 commonly used in transmission and reception and a low noise amplifier 43. The receiving RF signal from the low noise amplifier 43 is mixed with a local oscillation carrier from a local oscillator circuit 45 to generate a receiving IF (Intermediate Frequency) signal. Thus, ~~generated receiving IF signal is adjusted its~~the signal level of the generated IF signal is adjusted at an AGC amplifier 46, and then supplied to a base-band IC 47.

On the other hand, in transmitting, a transmitting IF signal generated in the base-band IC 47 is supplied to a mixer circuit 49 by way of an AGC amplifier 48, and the transmitting IF signal is converted to a transmitting RF signal by mixing a local oscillation carrier from a local oscillation circuit 50. This transmitting RF signal is transmitted from the antenna 41 by way of a power amplifier 51 and the frequency band separation filter 42. The base-band IC 47 functions to demodulate and decode the receiving IF signal to be an output audio signal in the receiving case~~,~~ and encode and modulate the~~an~~ input audio signal to be the transmitting IF signal in the transmitting case.

In the RF front-end part of the CDMA~~,~~ type mobile telephone apparatus of the construction, the gain control circuit having a plurality of stages in the second embodiment~~,~~ as mentioned above~~,~~ can be applied to the AGC amplifier 48, wherein the AGC amplifier 48 is supplied with the transmitting IF signal to be supplied to the mixer circuit 49 and must have a wide gain control range.

As thus described in the transmission stage of the CDMA~~,~~ type mobile telephone apparatus, a wide gain control characteristic having an extended linear range can be obtained by using the gain control circuit of the second embodiment as the AGC amplifier 48. Accordingly~~,~~ only the reduced ~~number of variable gain circuits are~~numbers of variable gain circuits are necessary in the transmission stage of the CDMA type mobile telephone apparatus and a power consumption of the mobile terminal can be achieved by applying the present invention.

In addition, the CDMA~~,~~ type mobile telephone apparatus is explained ~~for~~ as an example. However, the present invention is not limited to this application example but can be applied to various types of radio communication apparatuses.

ABSTRACT OF THE DISCLOSURE

A gain control circuit comprises a variable gain circuit having a predetermined gain control range and a control voltage supply circuit for supplying an internal control voltage to the variable gain circuit as a gain control signal. In this gain control circuit, the control voltage supply circuit generates the internal control voltage in response to an external control voltage so as to compensate ~~a~~ the linearity of the variable gain circuit to ~~an~~ the extent of the external control voltage where the variable gain circuit loses ~~a~~ linearity. This gain control circuit is applied to an AGC circuit of ~~a~~ the transmitting stage in a CDMA- type mobile phone.

English translation of drawing sheet

FIG. 1

11, a variable gain circuit

14 & 17, buffer amplifier

There is no in Fig.2

Fig.3A

Vc, internal control voltage

The present invention

Conventional embodiment

Fig.3B

VC, external control voltage

gain (dB)

linear range

The present invention

Conventional embodiment

Fig.4

35, control voltage supply circuit

31,32 & 33, a variable gain circuit

Fig.5

42, a band separation filter

46 & 48, AGC

Fig.6

108, control voltage supply circuit

47, baseband IC

Fig.7

Transmission gain (d B)

VC, external control voltage